

CLAIMS

What is claimed is:

1. An apparatus comprising:

2 a first drain bias network having an input suitable to couple to a FLASH cell;

3 a second drain bias network having an input suitable to couple to a FLASH cell;

4 and

5 an equalization circuit having a first node coupled to the input of the first drain

6 bias network and having a second node coupled to the input of the second drain bias

7 network and having a control signal to control operation of the equalization circuit.

1 2. The apparatus of claim 1 further comprising:

2 a sense amplifier having a first input, a second input, and an output; and

3 wherein:

4 the first drain bias network has an output coupled to the first input of the sense

5 amplifier and the second drain bias network has an output coupled to the second input

6 of the sense amplifier.

1 3. The apparatus of claim 2 further comprising:

2 a reference FLASH cell coupled to the second drain bias network; and

3 a FLASH cell coupled to the first drain bias network.

1       4. The apparatus of claim 3 wherein:  
2           the reference FLASH cell coupled to the second drain bias network through a  
3           reference column select transistor and the FLASH cell selectively coupled to the first  
4           drain bias network through a column select transistor, the column select transistor  
5           controlled by a column select signal.

1       5. The apparatus of claim 2 further comprising:  
2           a FLASH cell coupled to the first drain bias network.

1       6. The apparatus of claim 5 wherein:  
2           the FLASH cell selectively coupled to the first drain bias network through a first  
3           column select transistor.

1       7. The apparatus of claim 6 further comprising:  
2           a reference FLASH cell coupled through a second column select transistor to the  
3           second drain bias network.

1       8. The apparatus of claim 7 wherein:  
2           the equalization circuit is a transistor having a first node coupled to the input of  
3           the first drain bias network and having a second node coupled to the input of the  
4           second drain bias network and having a control electrode coupled to a third node of the  
5           transistor, the control electrode to deliver the control signal.

1        9. The apparatus of claim 4 wherein:  
2            the equalization circuit is a transistor having a first node coupled to the input of  
3            the first drain bias network and having a second node coupled to the input of the  
4            second drain bias network and having a control electrode coupled to a third node of the  
5            transistor, the control electrode to deliver the control signal.

1        10. The apparatus of claim 2 further comprising:  
2            a reference FLASH cell coupled to the second drain bias network.

1        11. The apparatus of claim 10 wherein:  
2            the reference FLASH cell coupled to the second drain bias network through a  
3            reference column select transistor.

1        12. A method comprising:  
2            equalizing a sense input and a reference input;  
3            coupling the sense input to a FLASH cell to be sensed;  
4            terminating equalization of the sense input and the reference input; and  
5            measuring a sense voltage, the sense voltage corresponding to the sense input.

1        13. The method of claim 12 further comprising:  
2            selecting the FLASH cell.

1        14. The method of claim 13 wherein:  
2                coupling further includes loading the FLASH cell with a load.

1        15. The method of claim 14 further comprising:  
2                coupling the reference input to a reference FLASH cell, including loading the  
3                reference FLASH cell;  
4                measuring a reference voltage, the reference voltage corresponding to the  
5                reference input; and  
6                comparing the sense voltage and the reference voltage.

1        16. An apparatus comprising:  
2                a first bias means for biasing a FLASH cell, the first bias means having an input  
3                and an output;  
4                a second bias means for biasing a reference FLASH cell, the second bias means  
5                having an input and an output; and  
6                an equalization means for selectively equalizing the input of the first bias means  
7                and the input of the second bias means, the equalization means coupled to the input of  
8                the first bias means and coupled to the input of the second bias means.

1        17. The apparatus of claim 16 further comprising:  
2                a comparison means for comparing the output of the first bias means and the  
3                output of the second bias means.

1        18. The apparatus of claim 17 further comprising:  
2            a FLASH cell selectively coupled to the input of the first bias means; and  
3            a reference FLASH cell coupled to the input of the second bias means.

1        19. The apparatus of claim 18 wherein:  
2            the input of the first bias means is disposed at a first node of the first bias means  
3            and the output of the first bias means is also disposed at the first node of the first bias  
4            means; and  
5            the input of the second bias means is disposed at a first node of the second bias  
6            means and the output of the second bias means is also disposed at the first node of the  
7            second bias means.

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1        20. A FLASH device comprising:

2            a FLASH cell array;

3            a control circuit block coupled to the FLASH cell array to control the FLASH cell

4            array; and

5            a comparison circuit block coupled to the FLASH cell array and coupled to the

6            control circuit block, the control circuit block to control the comparison circuit, the

7            comparison circuit including:

8            a first drain bias network having an input suitable to couple to a FLASH cell,

9            a second drain bias network having an input suitable to couple to a FLASH cell,

10          and

11          an equalization circuit having a first node coupled to the input of the first drain

12          bias network and having a second node coupled to the input of the second drain bias

13          network and having a control signal to control operation of the equalization circuit..

1        21. The FLASH device of claim 20, further comprising:

2            a sense amplifier having a first input, a second input, and an output; and

3        wherein:

4            the first drain bias network has an output coupled to the first input of the sense

5        amplifier and the second drain bias network has an output coupled to the second input

6        of the sense amplifier.

1        22. The FLASH device of claim 21 further comprising:  
2            a reference FLASH cell coupled through a column select transistor to the input of  
3        the second drain bias network; and wherein:  
4            a selected FLASH cell of the FLASH cell array selectively coupled through a  
5        column select transistor to the input of the first drain bias network.

1        23. The FLASH device of claim 22 further comprising:  
2            a power supply circuit coupled to the control circuit block and to the FLASH cell  
3        array and to the comparison circuit block.

1        24. An apparatus comprising:  
2            a first bias network having an input suitable to couple to a persistent memory  
3        storage location;  
4            a second bias network having an input suitable to couple to a persistent memory  
5        storage location; and  
6            an equalization circuit having a first node coupled to the input of the first bias  
7        network and having a second node coupled to the input of the second bias network and  
8        having a control signal to control operation of the equalization circuit.

1        25. The apparatus of claim 24 further comprising:  
2            a sense amplifier having a first input, a second input, and an output; and  
3        wherein:  
4            the first bias network has an output coupled to the first input of the sense  
5        amplifier and the second bias network has an output coupled to the second input of the  
6        sense amplifier, the output of the first bias network having a relationship with the input  
7        of the first bias network, the output of the second bias network having a relationship  
8        with the input of the second bias network.

1        26. The apparatus of claim 25 further comprising:  
2            a reference persistent memory storage location coupled to the second bias  
3        network through a reference column select circuit and a persistent memory storage  
4        location selectively coupled to the first bias network through a column select circuit, the  
5        column select circuit controlled by a column select signal.

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